

PIC18F2455/2550/4455/4550

REGISTER 25-4: CONFIG2H: CONFIGURATION REGISTER 2 HIGH (BYTE ADDRESS 300003h)

U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN
bit 7							bit 0

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS3:WDTPS0:** Watchdog Timer Postscale Select bits

1111 = 1:32,768

1110 = 1:16,384

1101 = 1:8,192

1100 = 1:4,096

1011 = 1:2,048

1010 = 1:1,024

1001 = 1:512

1000 = 1:256

0111 = 1:128

0110 = 1:64

0101 = 1:32

0100 = 1:16

0011 = 1:8

0010 = 1:4

0001 = 1:2

0000 = 1:1

bit 0 **WDTEN:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled (control is placed on the SWDTEN bit)

Este registro esta configurado con el valor = 0x1E en el firmware bootloader en el sistema Bolt 18F2550, es decir, el WDT está deshabilitado (pero puede habilitarse en el programa de aplicación por medio del bit SWDTEN)

El preescalador está a su máximo valor de 32768, equivalente a un timeout de 131 segundos. Al estar habilitado, el temporizador WDT genera un reset automático al microcontrolador al llegar su timeout (cuenta máxima). La función ClrWdt() de C18 reinicia a cero la cuenta del WDT.

25.2 Watchdog Timer (WDT)

For PIC18F2455/2550/4455/4550 devices, the WDT is driven by the INTRC source. When the WDT is enabled, the clock source is also enabled. The nominal WDT period is 4 ms and has the same stability as the INTRC oscillator.

The 4 ms period of the WDT is multiplied by a 16-bit postscaler. Any output of the WDT postscaler is selected by a multiplexer, controlled by bits in Configuration Register 2H. Available periods range from 4 ms to 131.072 seconds (2.18 minutes). The WDT and postscaler are cleared when any of the following events occur: a SLEEP or CLRWDT instruction is executed, the IRCF bits (OSCCON<6:4>) are changed or a clock failure has occurred.

Note 1: The CLRWDT and SLEEP instructions clear the WDT and postscaler counts when executed.

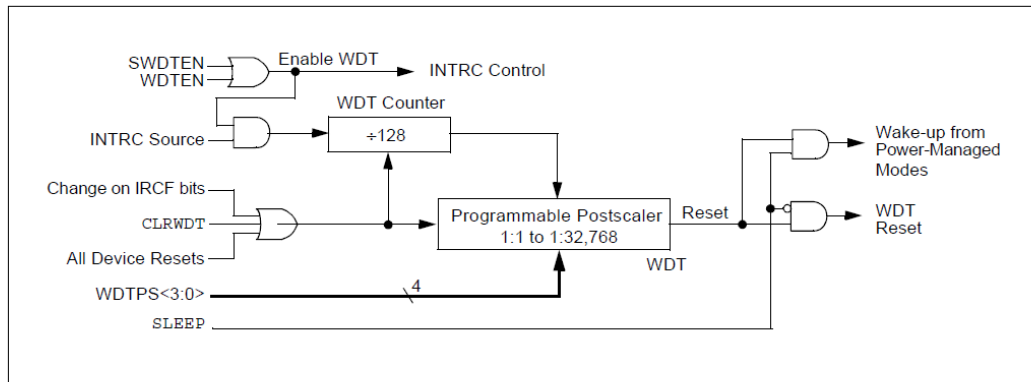
2: Changing the setting of the IRCF bits (OSCCON<6:4>) clears the WDT and postscaler counts.

3: When a CLRWDT instruction is executed, the postscaler count will be cleared.

25.2.1 CONTROL REGISTER

Register 25-15 shows the WDTCON register. This is a readable and writable register which contains a control bit that allows software to override the WDT enable Configuration bit, but only if the Configuration bit has disabled the WDT.

FIGURE 25-1: WDT BLOCK DIAGRAM



REGISTER 25-15: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SWDTEN ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'
 bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit⁽¹⁾
 1 = Watchdog Timer is on
 0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bit, WD TEN, is enabled.

TABLE 25-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
RCON	IPEN	SBOREN ⁽¹⁾	—	R \bar{I}	$\bar{T}O$	PD	POR	BOR	52
WDTCON	—	—	—	—	—	—	—	SWDTEN	52

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

Note 1: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.

REGISTER 4-1: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1 ⁽¹⁾	U-0	R/W-1	R-1	R-1	R/W-0 ⁽²⁾	R/W-0
IPEN	SBOREN	—	\overline{RI}	\overline{TO}	\overline{PD}	\overline{POR}	\overline{BOR}
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **IPEN:** Interrupt Priority Enable bit
 1 = Enable priority levels on interrupts
 0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)
- bit 6 **SBOREN:** BOR Software Enable bit⁽¹⁾
 If BOREN1:BOREN0 = 01:
 1 = BOR is enabled
 0 = BOR is disabled
 If BOREN1:BOREN0 = 00, 10 or 11:
 Bit is disabled and read as '0'.
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **\overline{RI} :** RESET Instruction Flag bit
 1 = The RESET instruction was not executed (set by firmware only)
 0 = The RESET instruction was executed causing a device Reset (must be set in software after a Brown-out Reset occurs)
- bit 3 **\overline{TO} :** Watchdog Time-out Flag bit
 1 = Set by power-up, CLRWDT instruction or SLEEP instruction
 0 = A WDT time-out occurred
- bit 2 **\overline{PD} :** Power-Down Detection Flag bit
 1 = Set by power-up or by the CLRWDT instruction
 0 = Set by execution of the SLEEP instruction
- bit 1 **\overline{POR} :** Power-on Reset Status bit⁽²⁾
 1 = A Power-on Reset has not occurred (set by firmware only)
 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
- bit 0 **\overline{BOR} :** Brown-out Reset Status bit
 1 = A Brown-out Reset has not occurred (set by firmware only)
 0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

- Note 1:** If SBOREN is enabled, its Reset state is '1'; otherwise, it is '0'.
Note 2: The actual Reset value of \overline{POR} is determined by the type of device Reset. See the notes following this register and Section 4.6 "Reset State of Registers" for additional information.

Note 1: It is recommended that the \overline{POR} bit be set after a Power-on Reset has been detected so that subsequent Power-on Resets may be detected.
Note 2: Brown-out Reset is said to have occurred when \overline{BOR} is '0' and \overline{POR} is '1' (assuming that \overline{POR} was set to '1' by software immediately after POR).